

<b>L Number</b>	<b>Hits</b>	<b>Search Text</b>	<b>DB</b>	<b>Time stamp</b>
<b>1</b>	<b>7880</b>	<b>associative near6 (cache memory storage)</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:04</b>
<b>2</b>	<b>119</b>	<b>((controller logic circuit) same multiplexer same (associative near6 (cache memory storage)))</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:21</b>
<b>3</b>	<b>43</b>	<b>(read\$3 load\$3) near4 (buffer register) and ((controller logic circuit) same multiplexer same (associative near6 (cache memory storage)))</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:21</b>
<b>5</b>	<b>14</b>	<b>(concurrently simultaneous parallel ("SAME" adj3 time)) same ((controller logic circuit) same multiplexer same (associative near6 (cache memory storage)))</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:20</b>
<b>6</b>	<b>84</b>	<b>(concurrently simultaneous parallel ("SAME" adj3 time)) and ((controller logic circuit) same multiplexer same (associative near6 (cache memory storage)))</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:21</b>
<b>7</b>	<b>513756</b>	<b>((controller logic circuit) same (concurrently simultaneous parallel ("SAME" adj3 time)))</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:21</b>
<b>8</b>	<b>38490</b>	<b>((controller logic circuit) same (concurrently simultaneous parallel ("SAME" adj3 time)) same enabl\$3)</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:22</b>
<b>9</b>	<b>272</b>	<b>(read\$3 load\$3) near4 (buffer register) and (associative near6 (cache memory storage)) and ((controller logic circuit) same (concurrently simultaneous parallel ("SAME" adj3 time)) same enabl\$3) and multiplexer</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:23</b>
<b>10</b>	<b>172</b>	<b>(read\$3 load\$3) near4 (buffer register) and (associative near6 (cache memory storage)) and ((controller logic circuit) same (concurrently simultaneous parallel ("SAME" adj3 time)) same enabl\$3) and (multiplexer with (input\$4 output\$4))</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:24</b>
<b>11</b>	<b>60</b>	<b>711/\$.ccls. and ((read\$3 load\$3) near4 (buffer register) and (associative near6 (cache memory storage)) and ((controller logic circuit) same (concurrently simultaneous parallel ("SAME" adj3 time)) same enabl\$3) and (multiplexer with (input\$4 output\$4)))</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT</b>	<b>2003/08/20 17:24</b>